

FIG. 1B

FIG. 1C

FIG. 1C^I

FIG. 1C^{II}

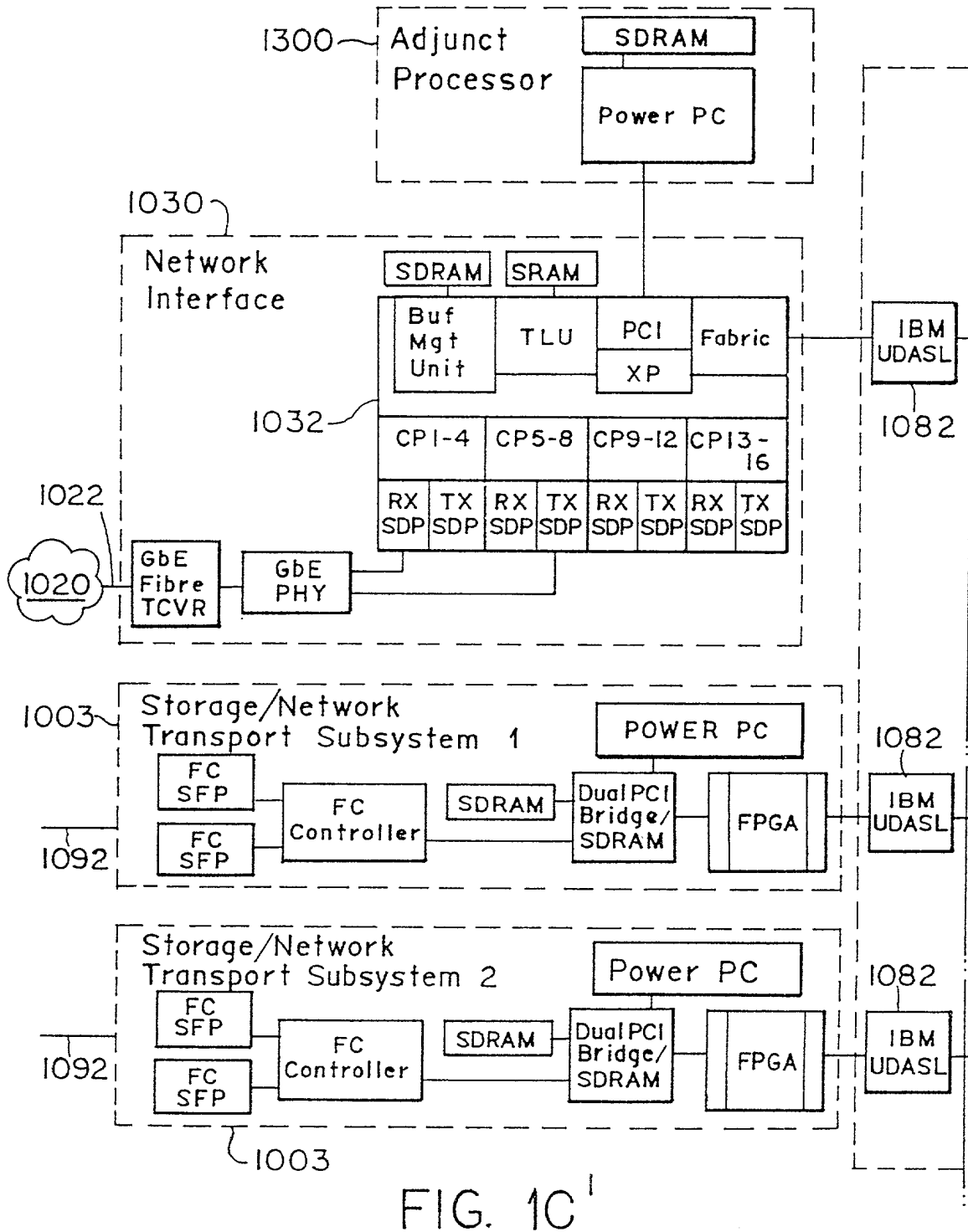


FIG. 1C^I

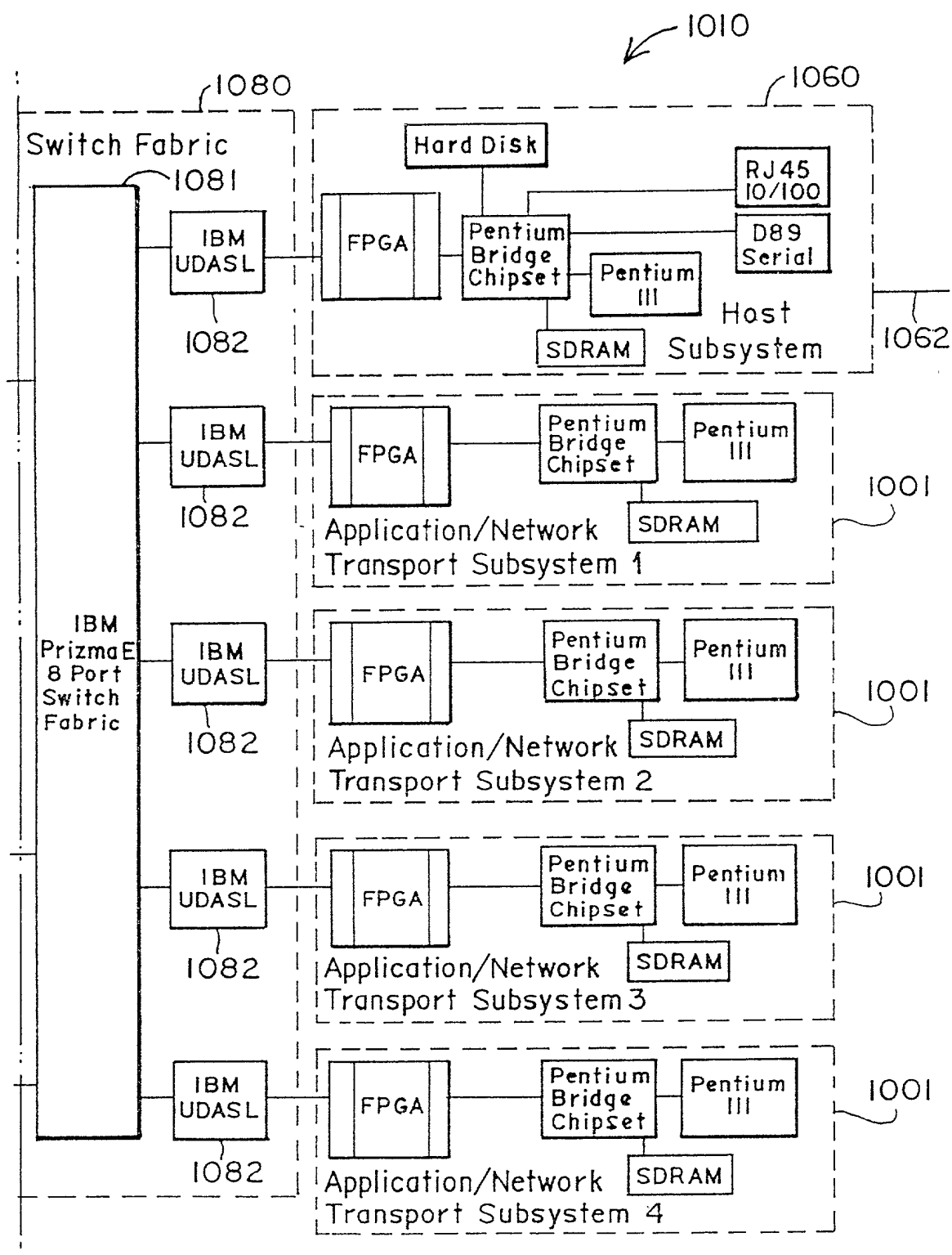


FIG. 1C¹¹

FIG. 1D

FIG. 1D^I

FIG. 1D^{II}

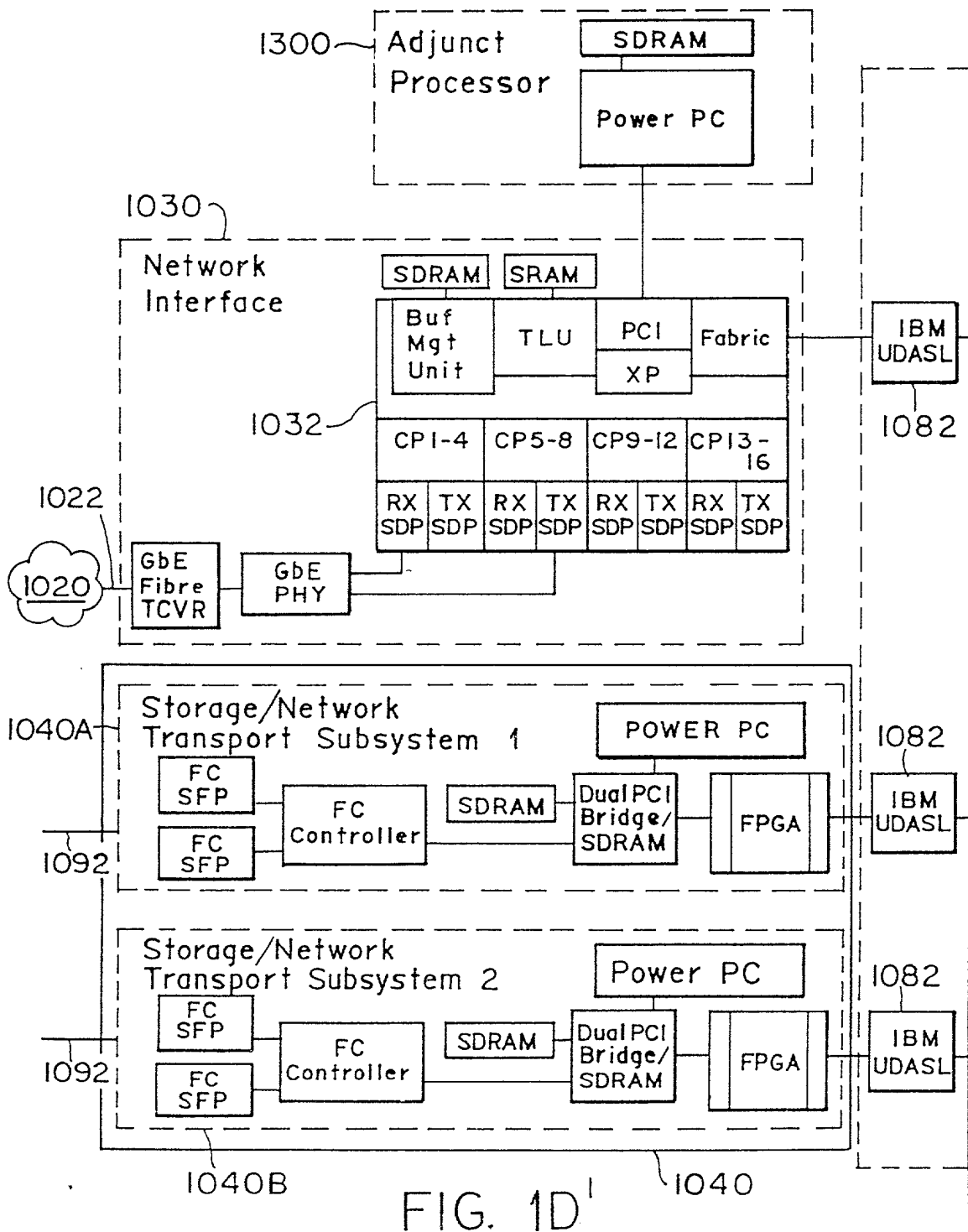


FIG. 1D^I

1040

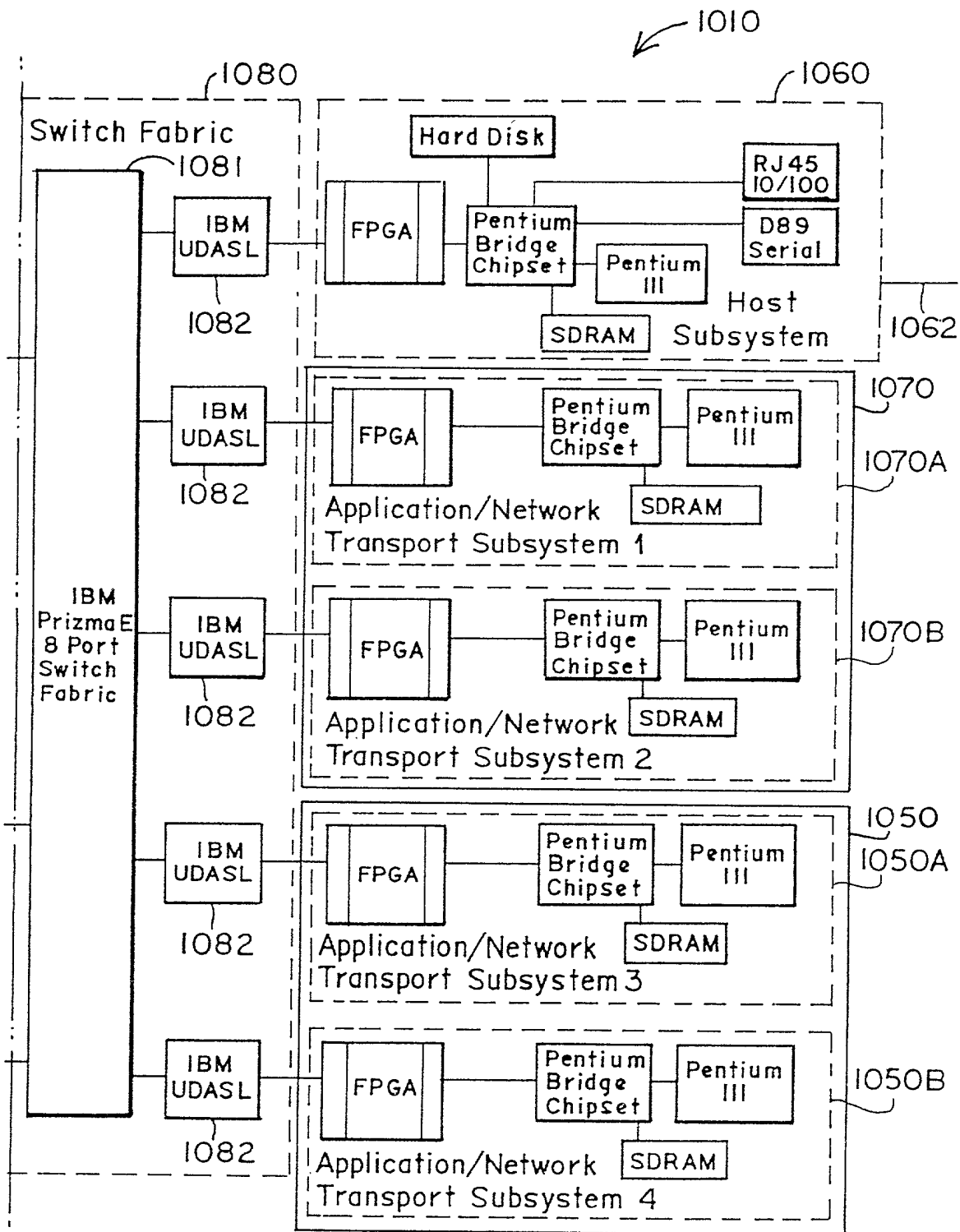


FIG. 1D^{II}

FIG. 1E

FIG. 1E^I

FIG. 1E^{II}

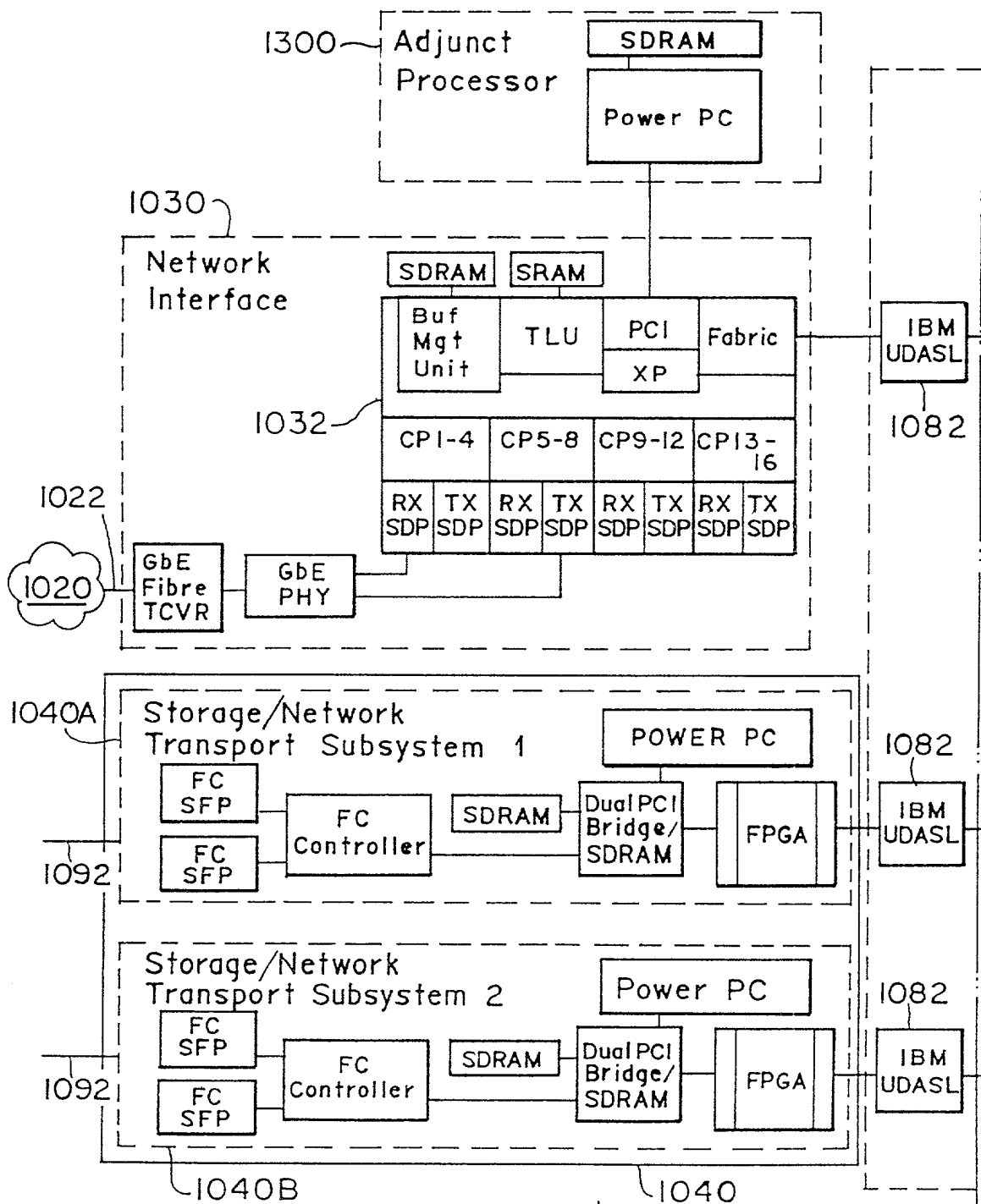


FIG. 1E^I

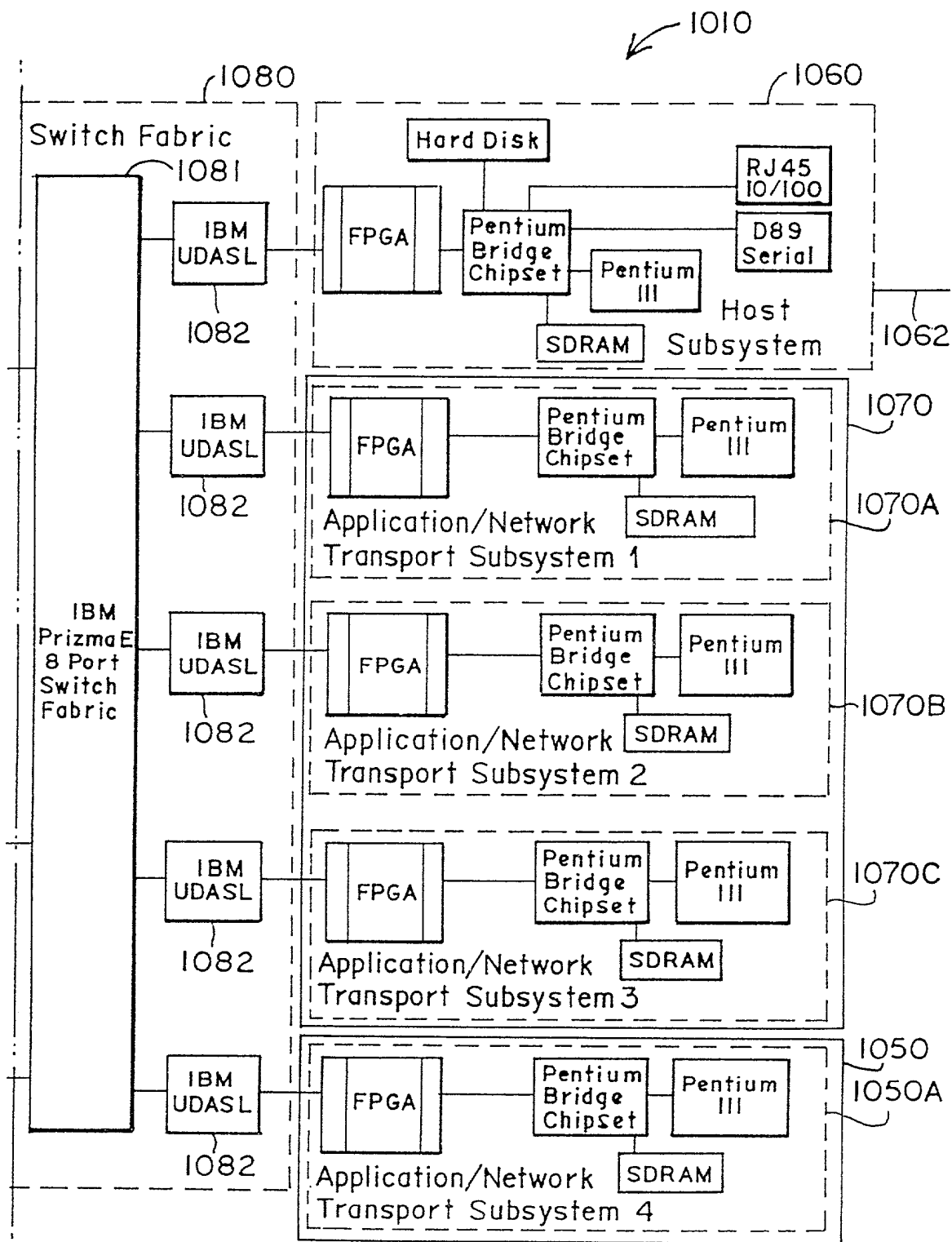


FIG. 1E¹¹

FIG. 1F

FIG. 1F^I

FIG. 1F^{II}

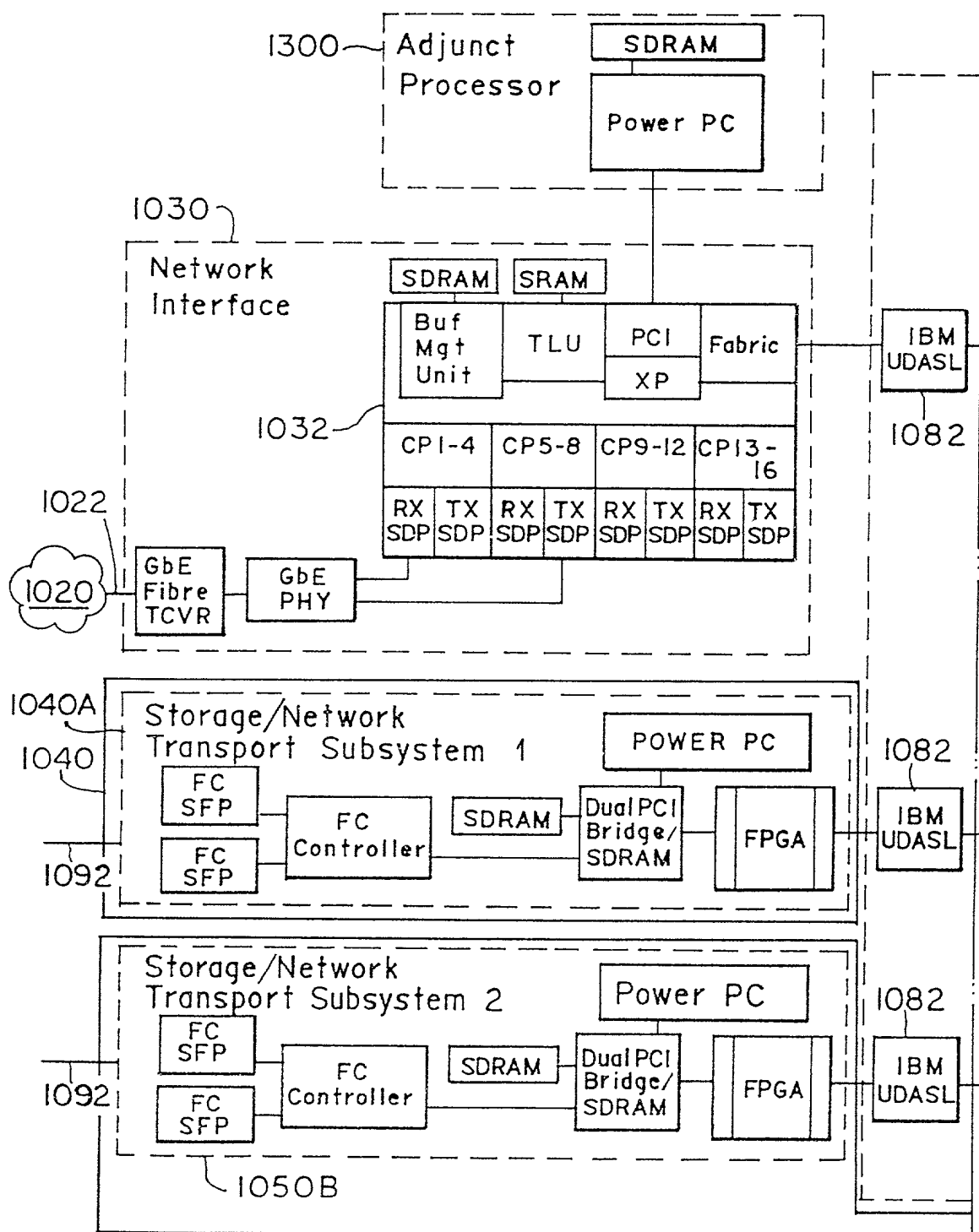


FIG. 1F^I

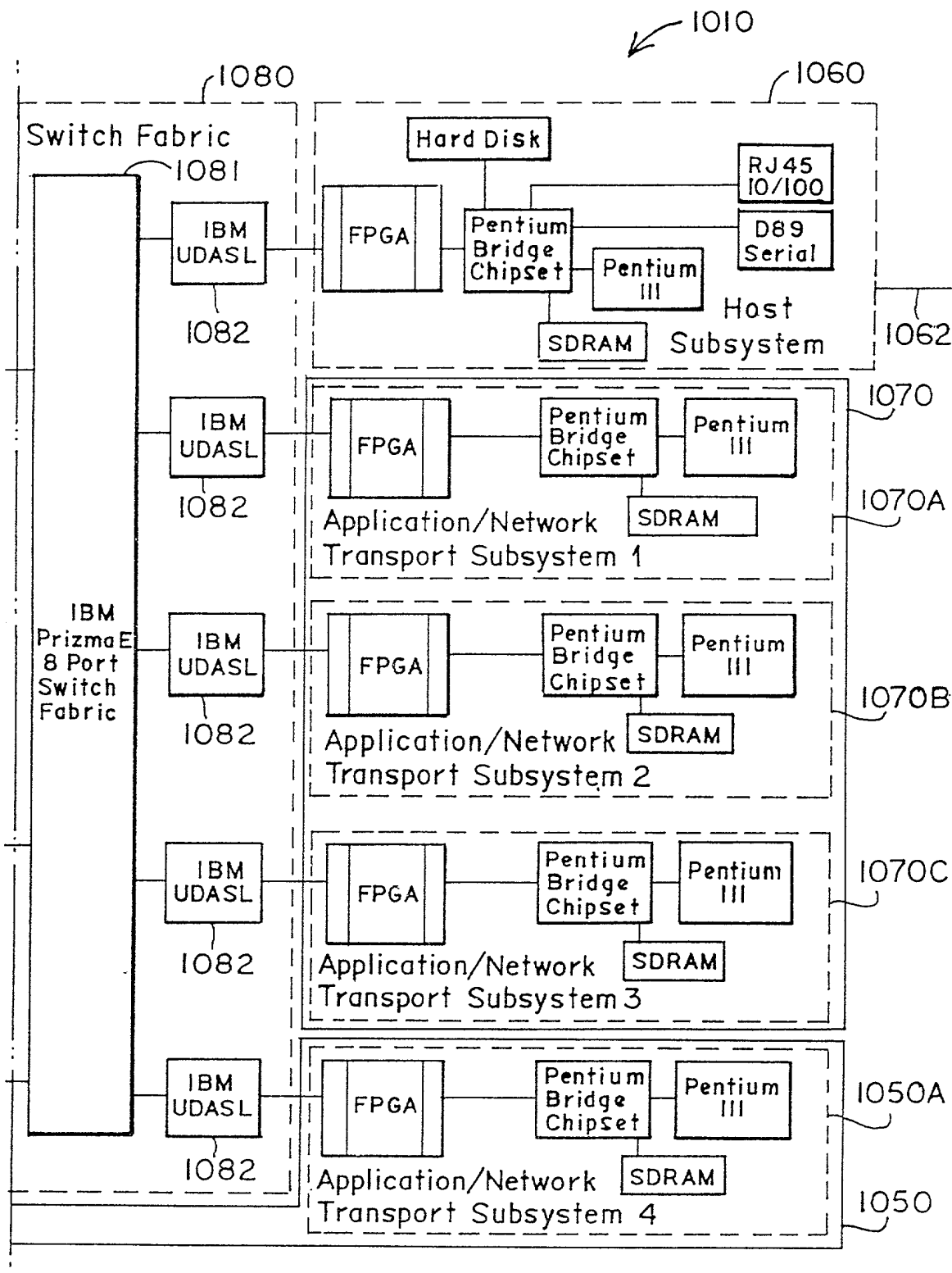


FIG. 1F^{II}

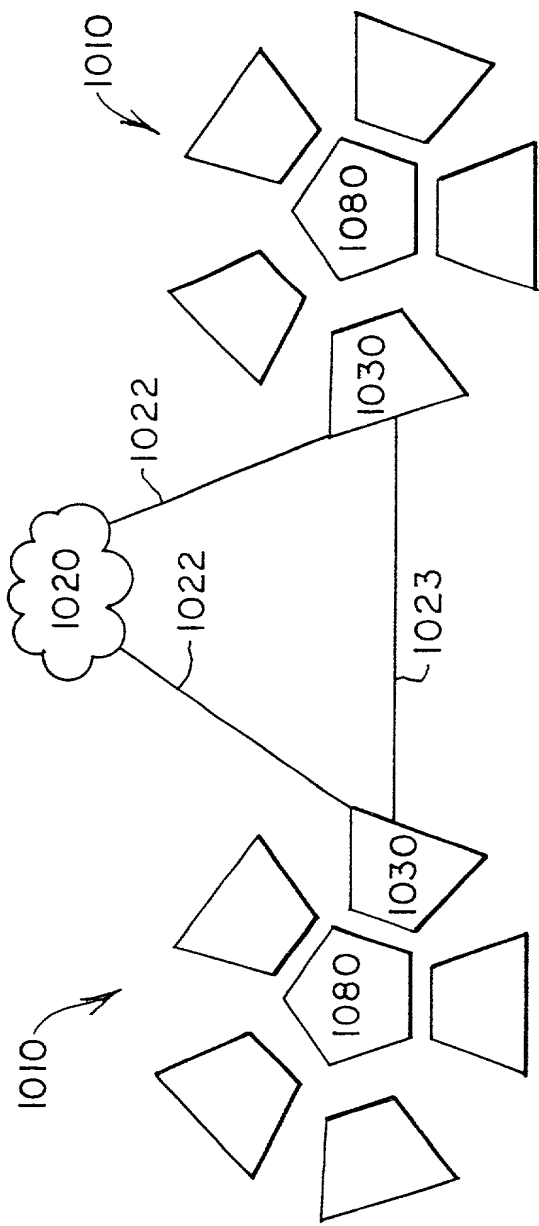


FIG. 1G

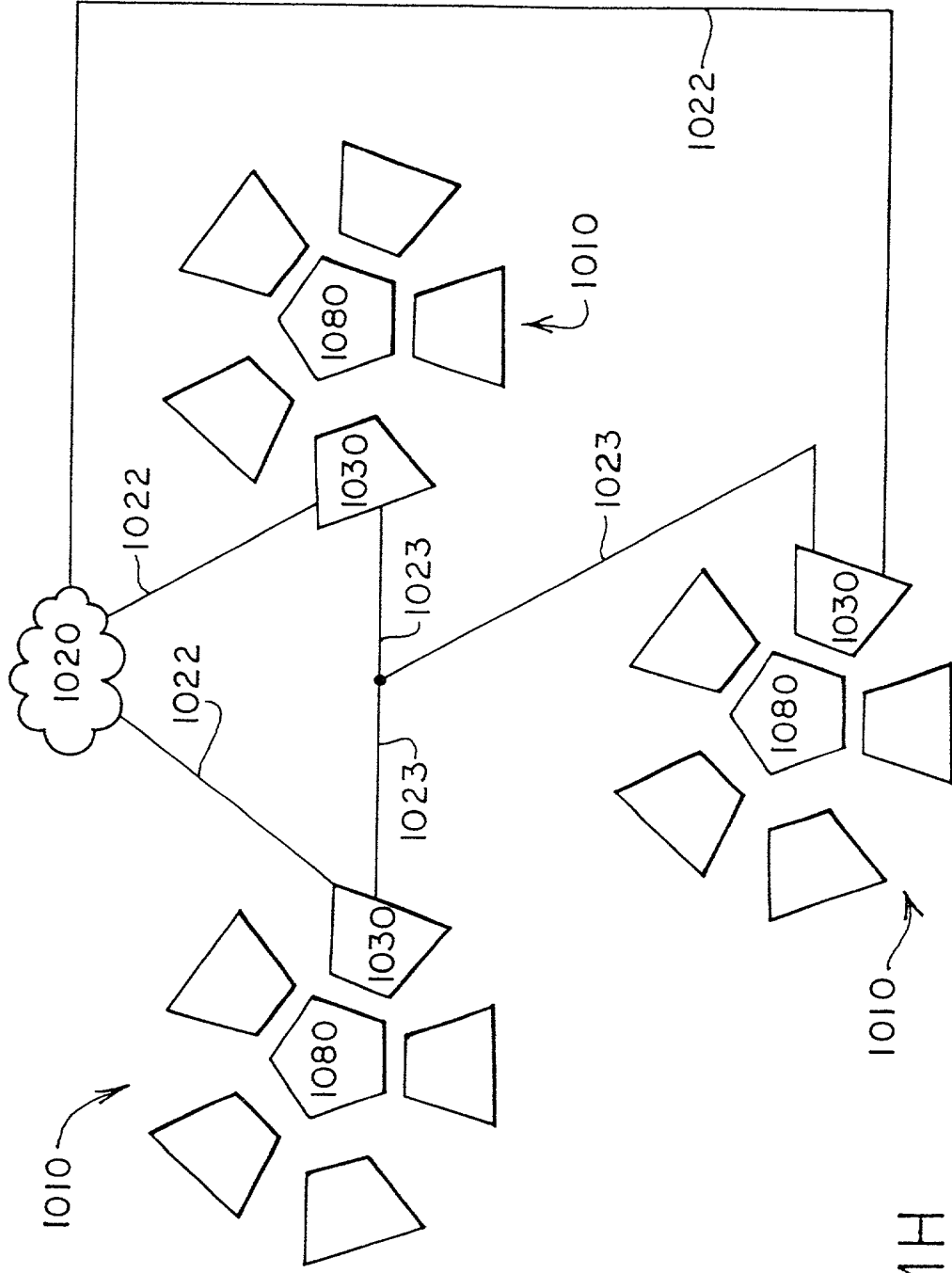


FIG. 1H

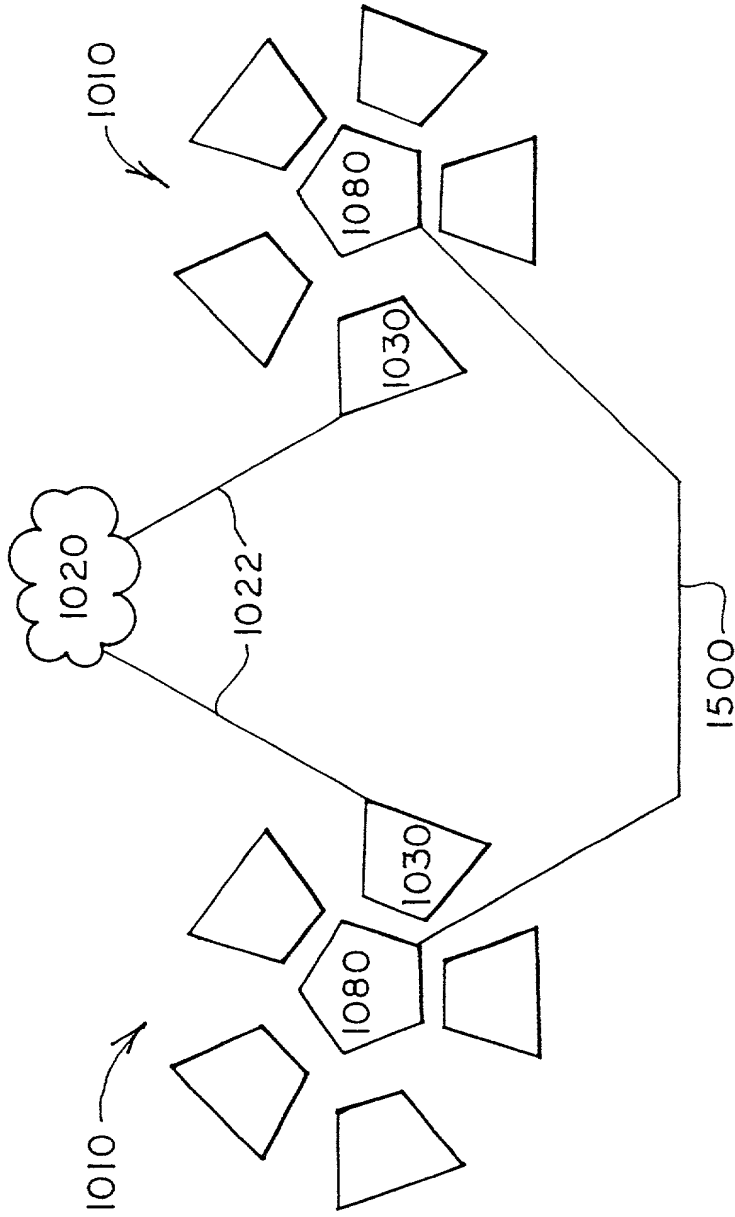


FIG. 10I

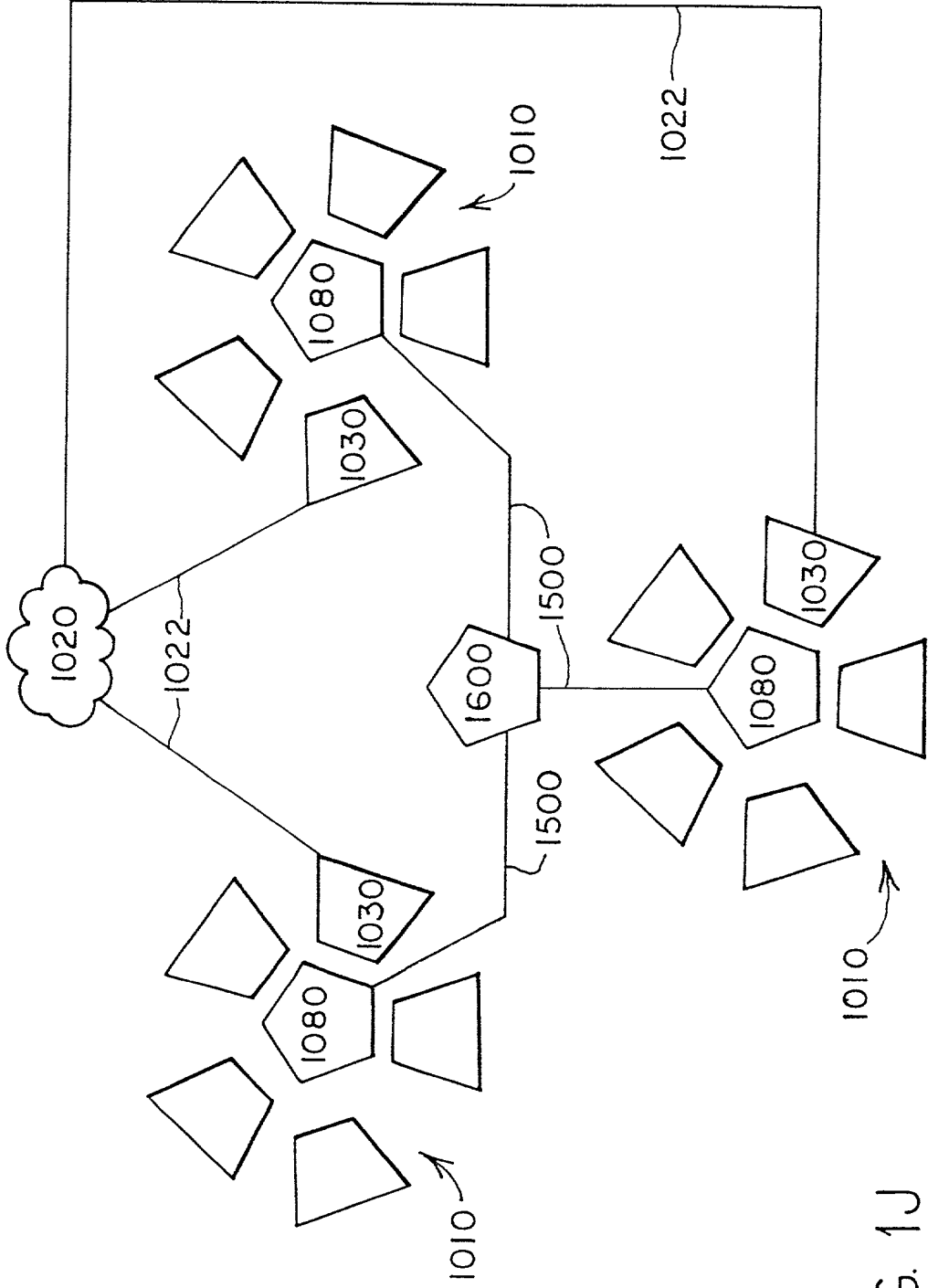


FIG. 1J

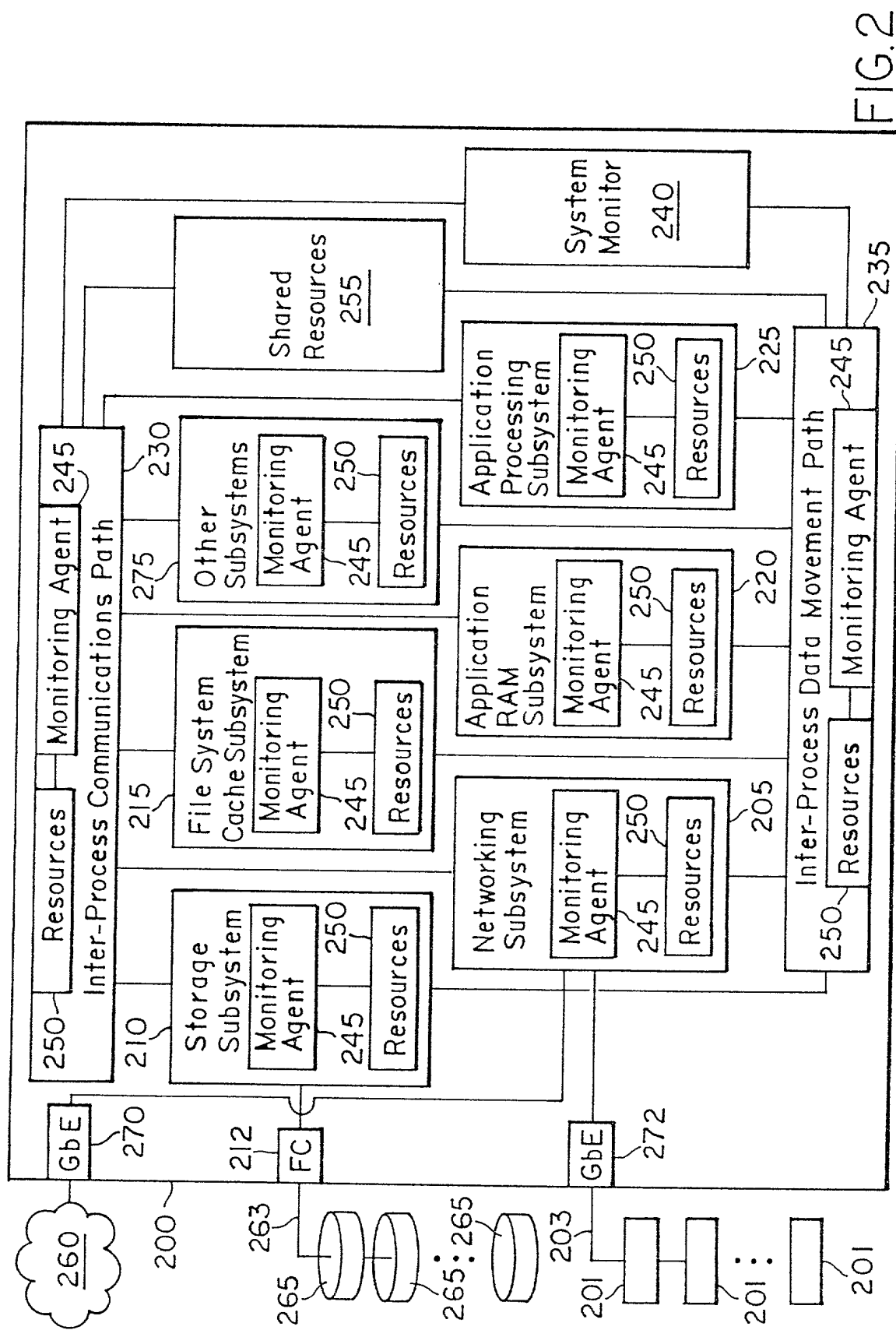
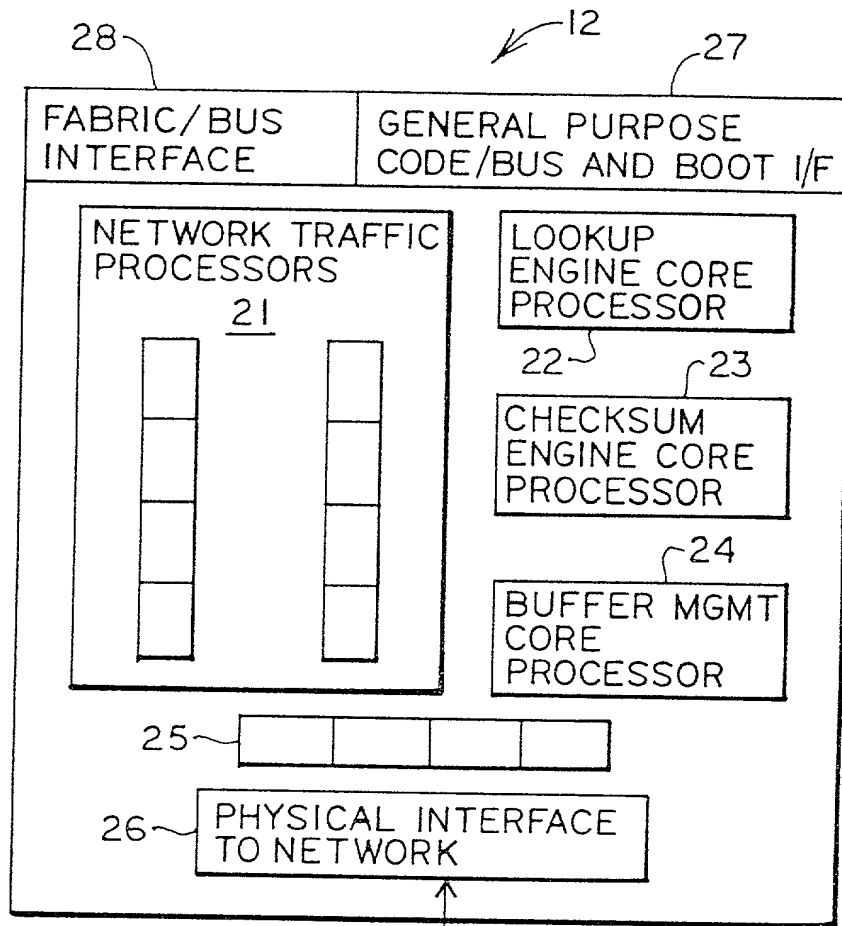


FIG. 3 is a block diagram of a network interface card (NIC) 12. The NIC 12 includes a FABRIC/BUS INTERFACE 28 and a GENERAL PURPOSE CODE/BUS AND BOOT I/F 27. The FABRIC/BUS INTERFACE 28 includes NETWORK TRAFFIC PROCESSORS 21, which are represented by two vertical columns of four rectangular blocks each. The GENERAL PURPOSE CODE/BUS AND BOOT I/F 27 includes a LOOKUP ENGINE CORE PROCESSOR 22, a CHECKSUM ENGINE CORE PROCESSOR 23, and a BUFFER MGMT CORE PROCESSOR 24. Below these components is a row of four rectangular blocks 25, and below that is a PHYSICAL INTERFACE TO NETWORK 26. A zigzag arrow points from the PHYSICAL INTERFACE TO NETWORK 26 to the text "TO ROUTER".



TO ROUTER

FIG. 3

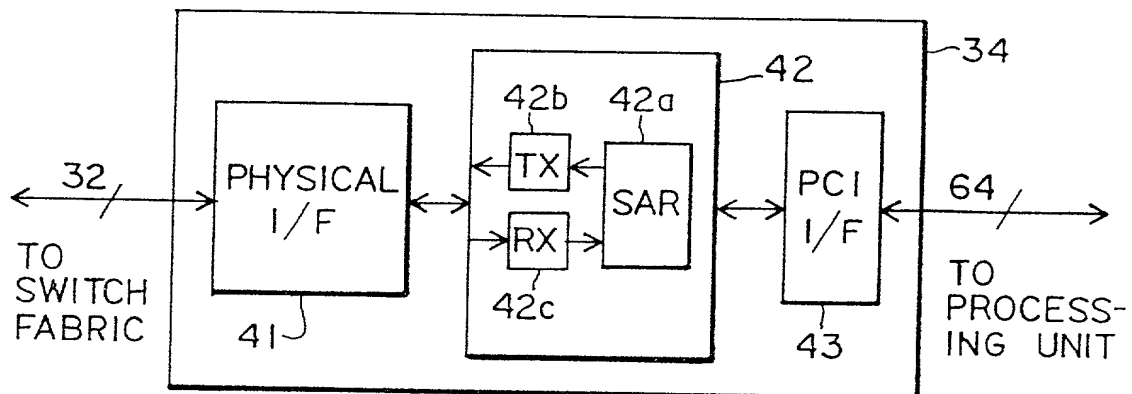


FIG. 4

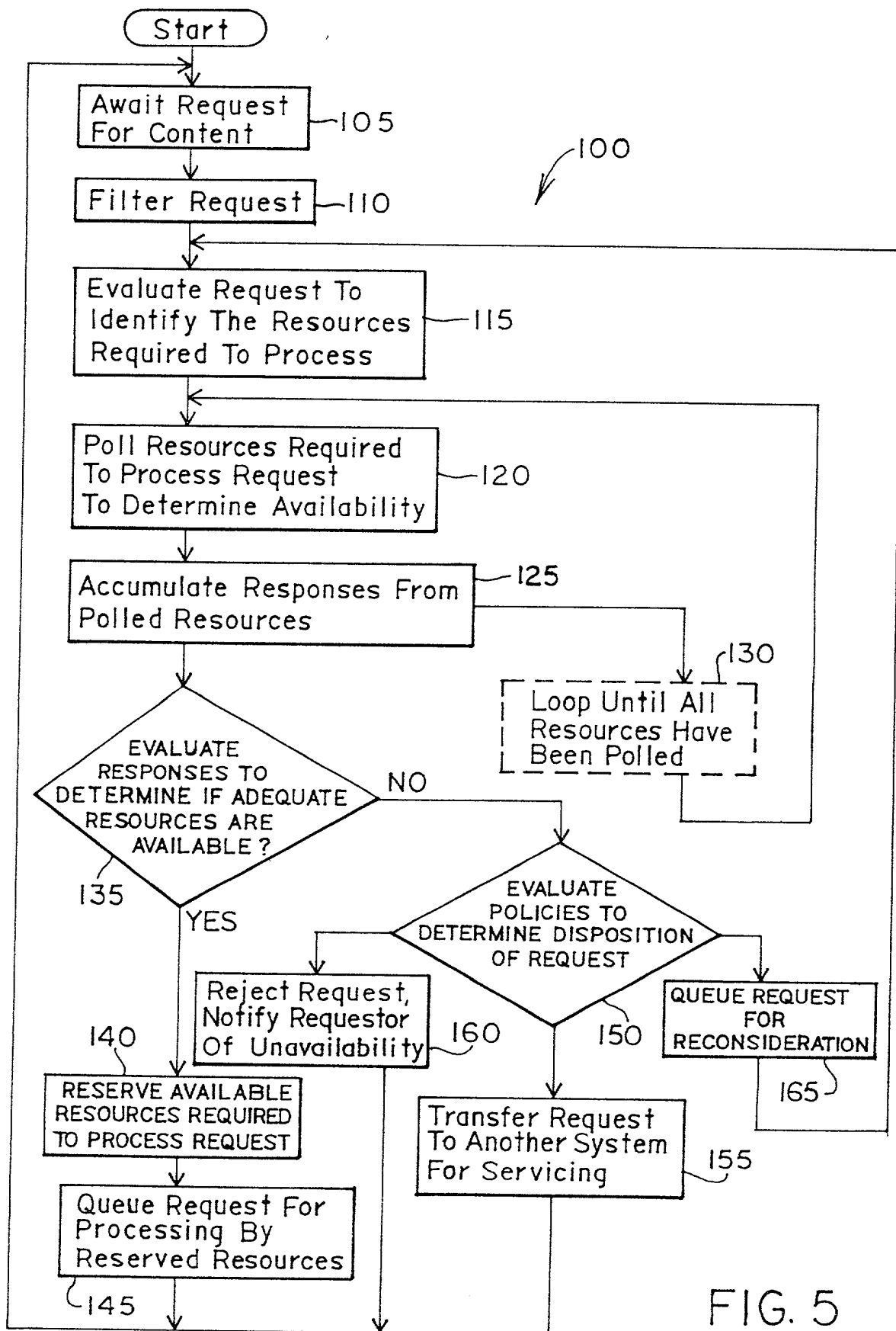


FIG. 5

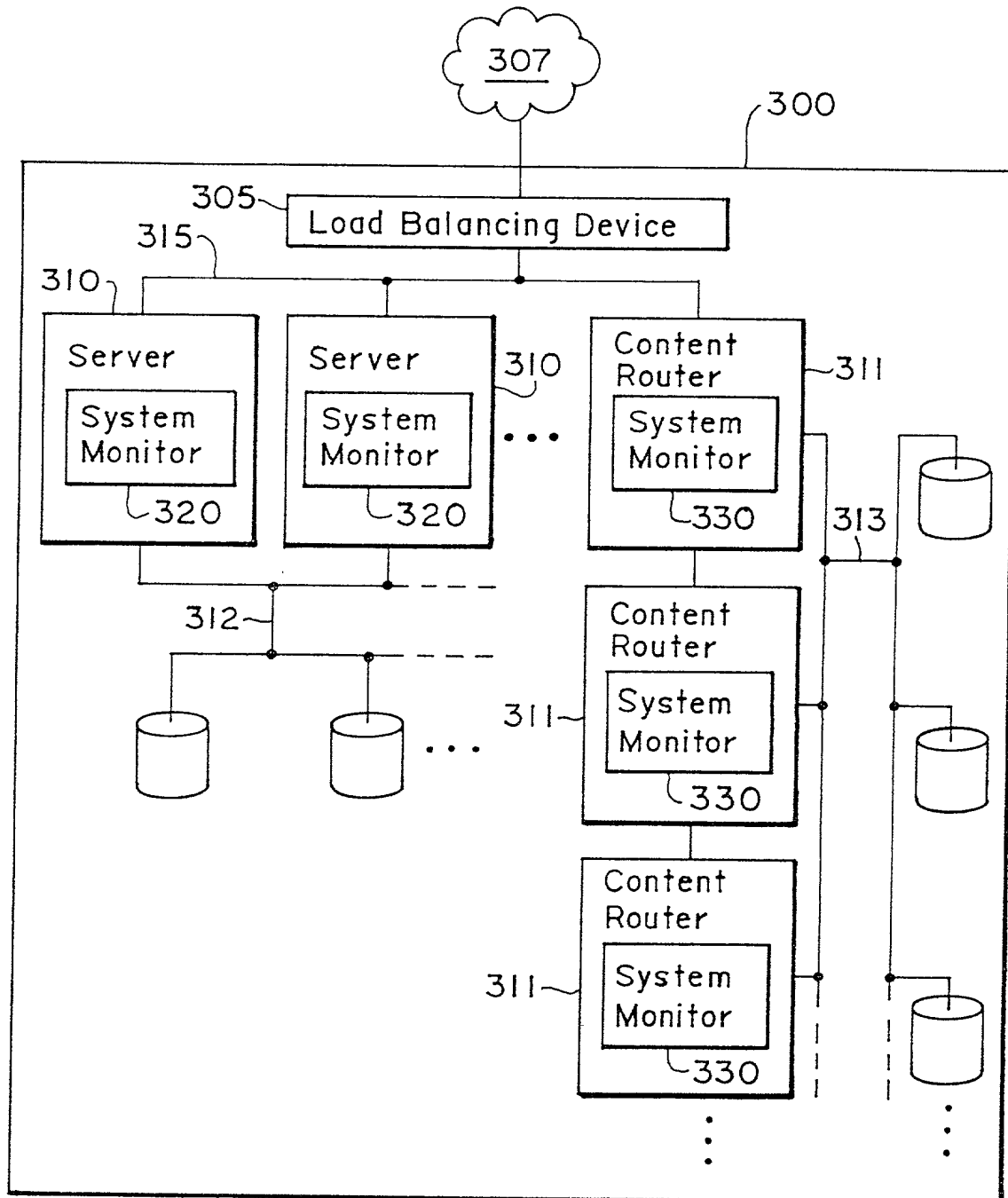


FIG. 6

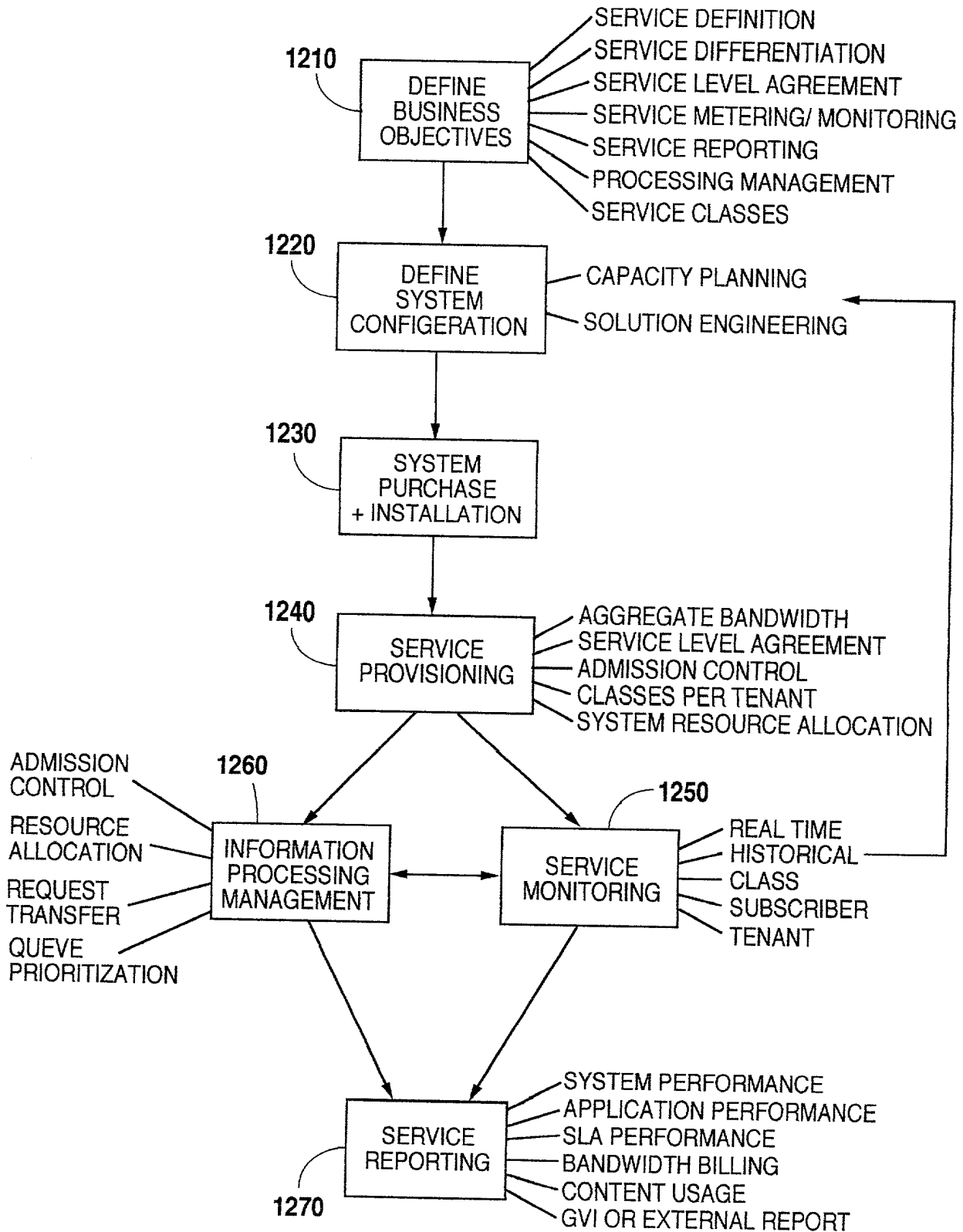


Fig. 8

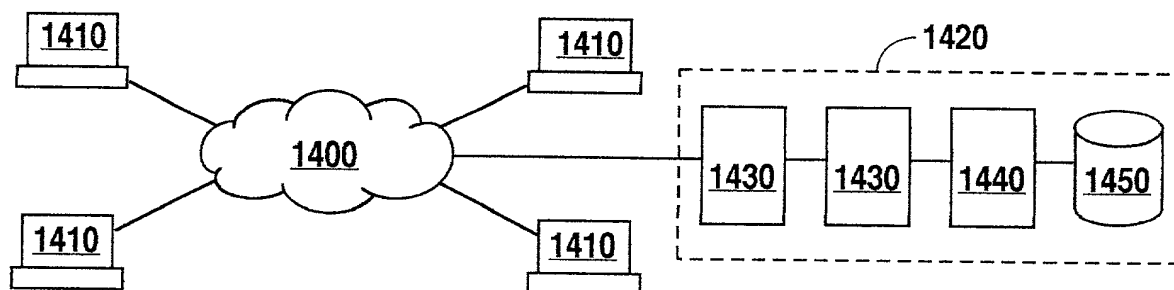


Fig. 9A

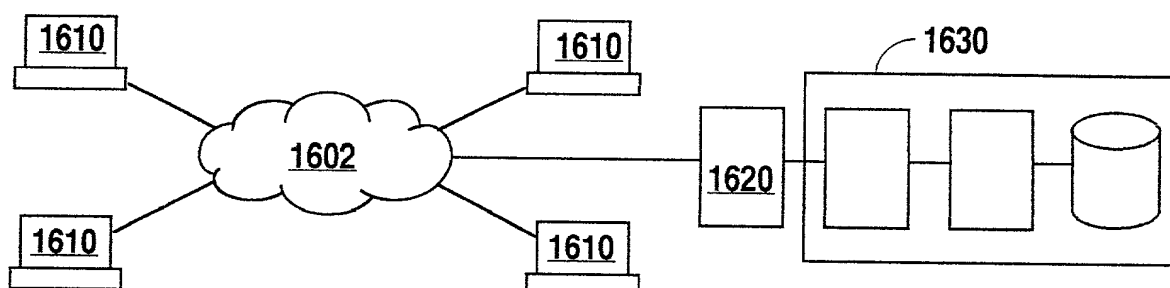


Fig. 9B

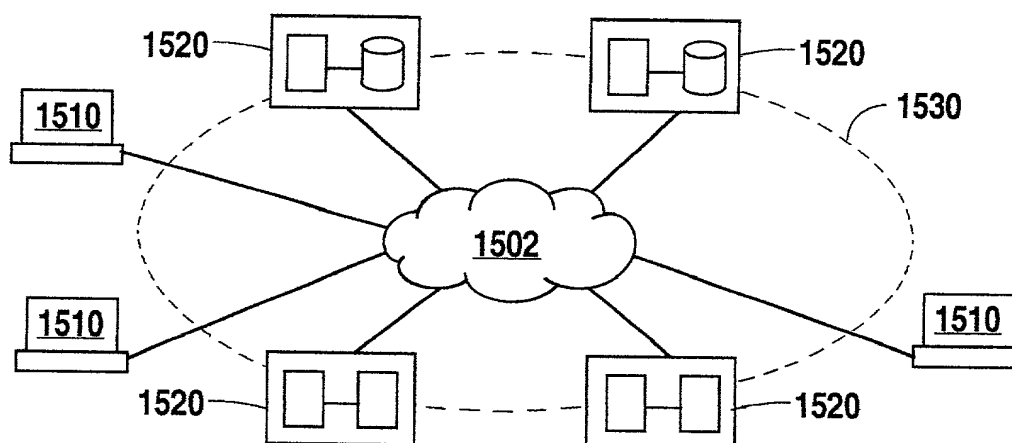


Fig. 9C

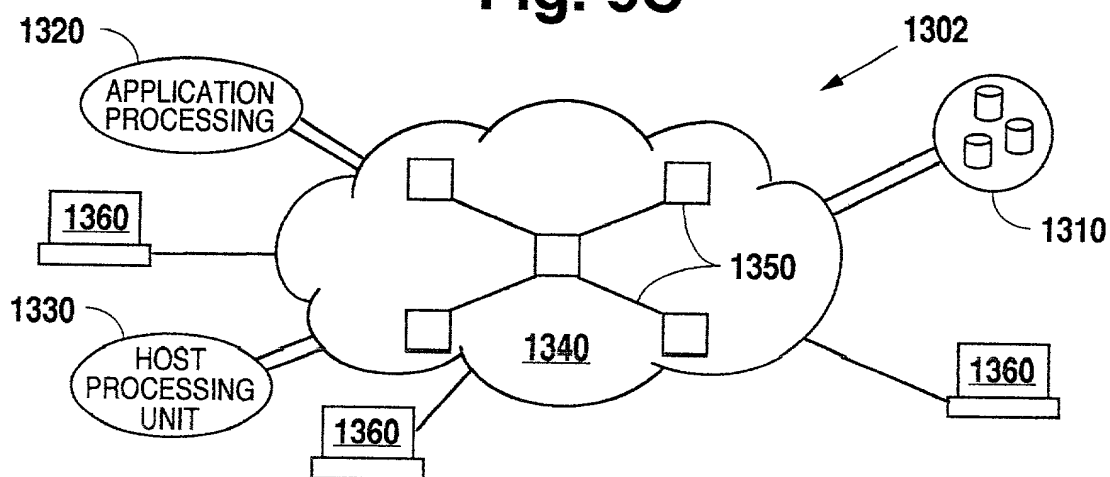


Fig. 9D

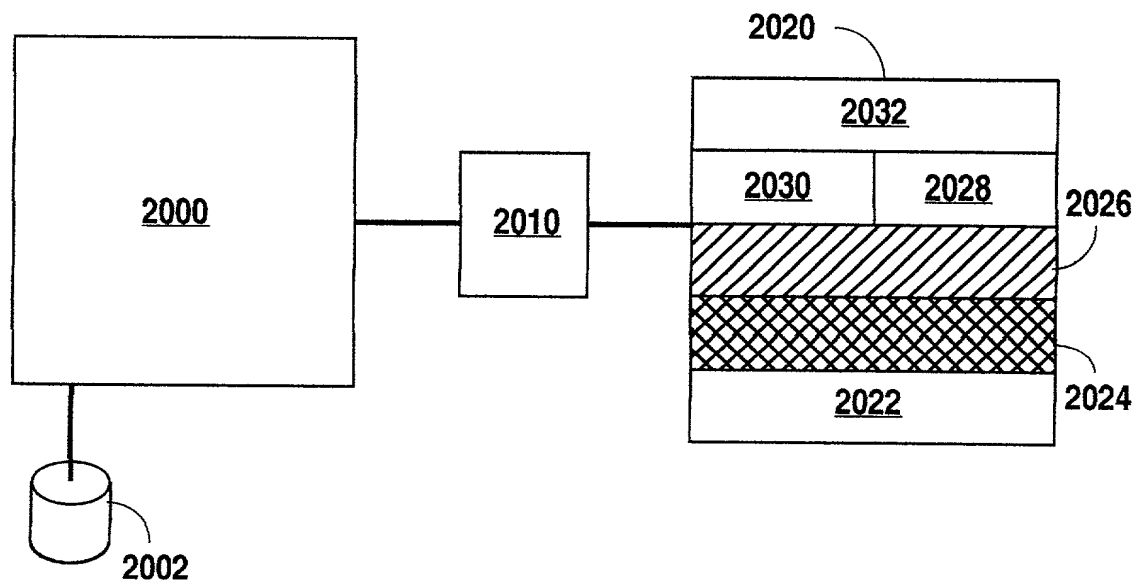


Fig. 10

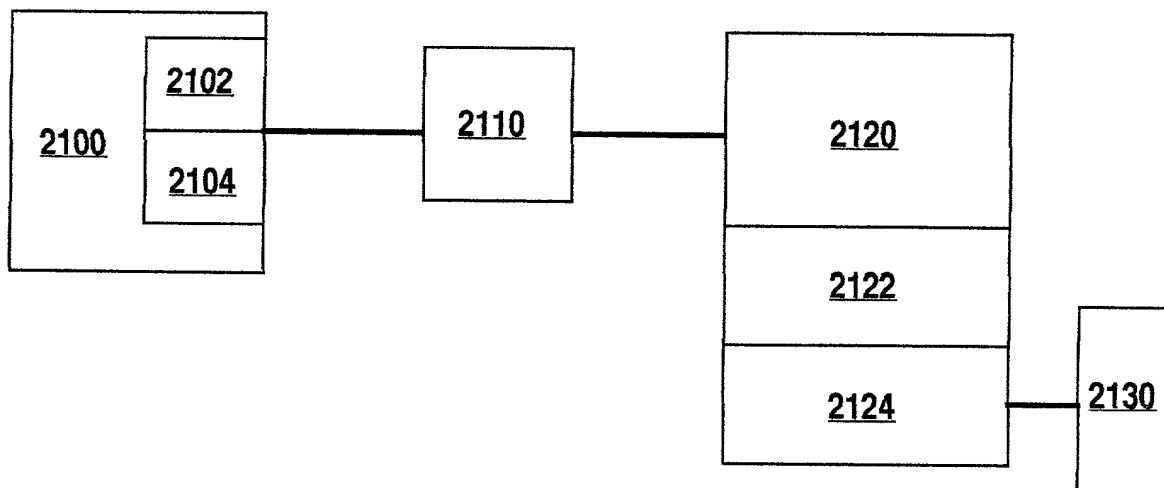


Fig. 11

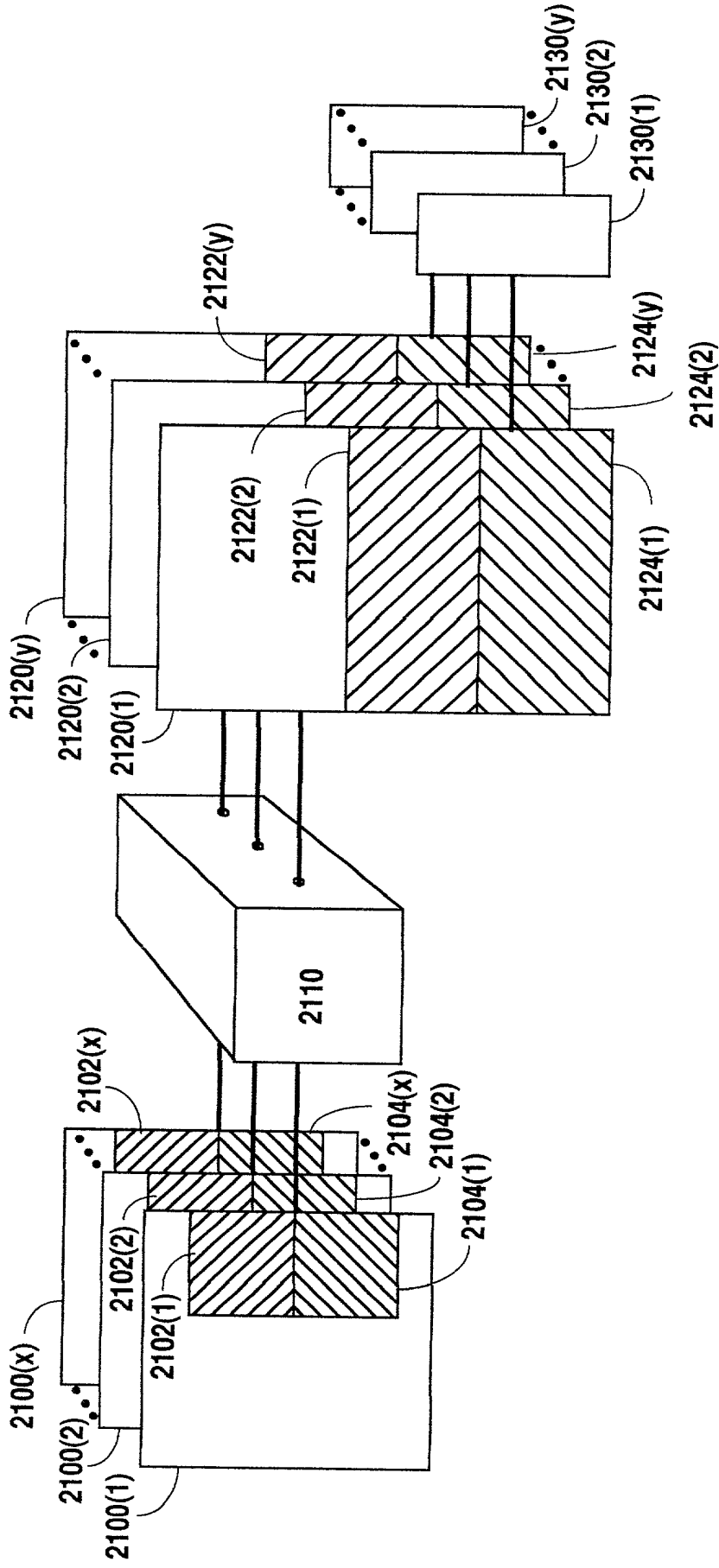


Fig. 12

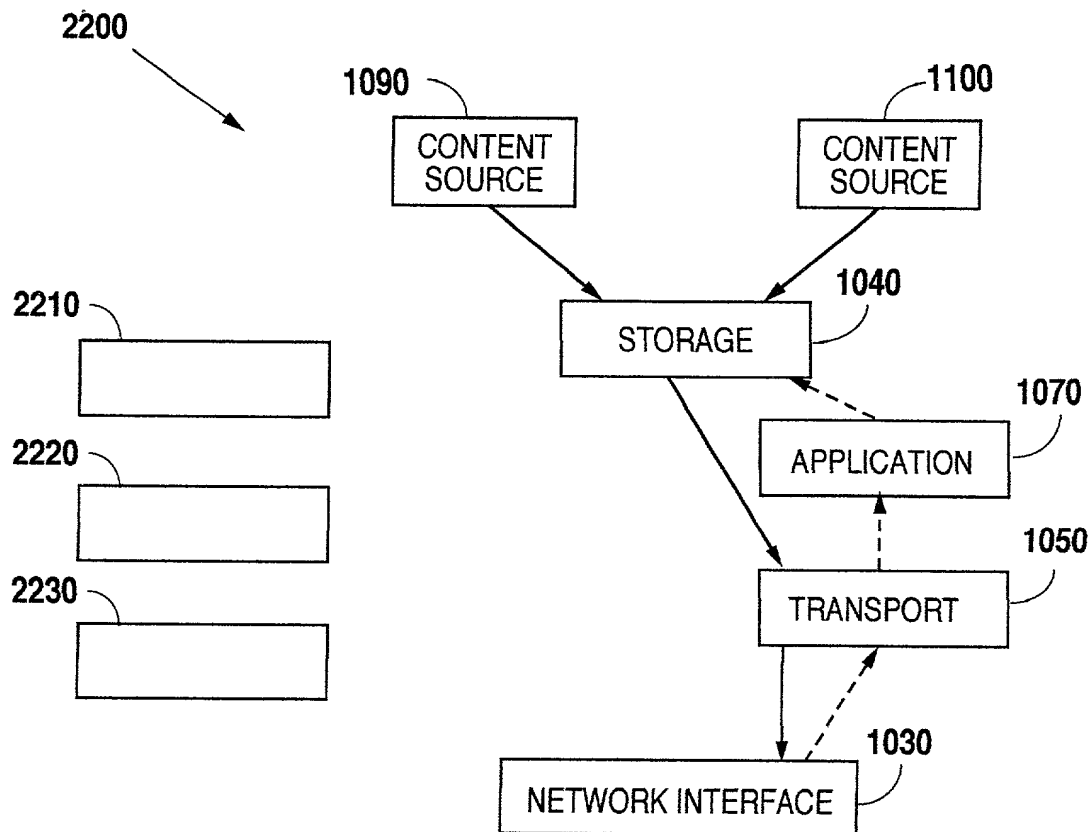


Fig. 13

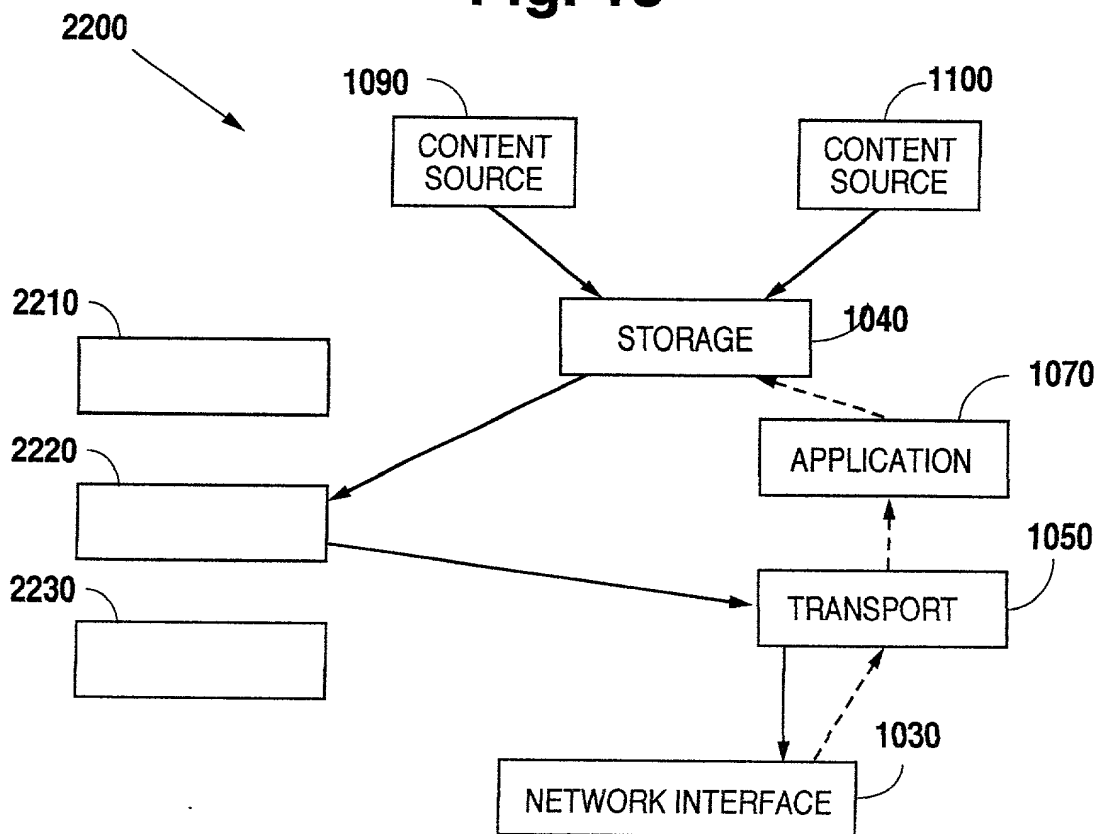


Fig. 14

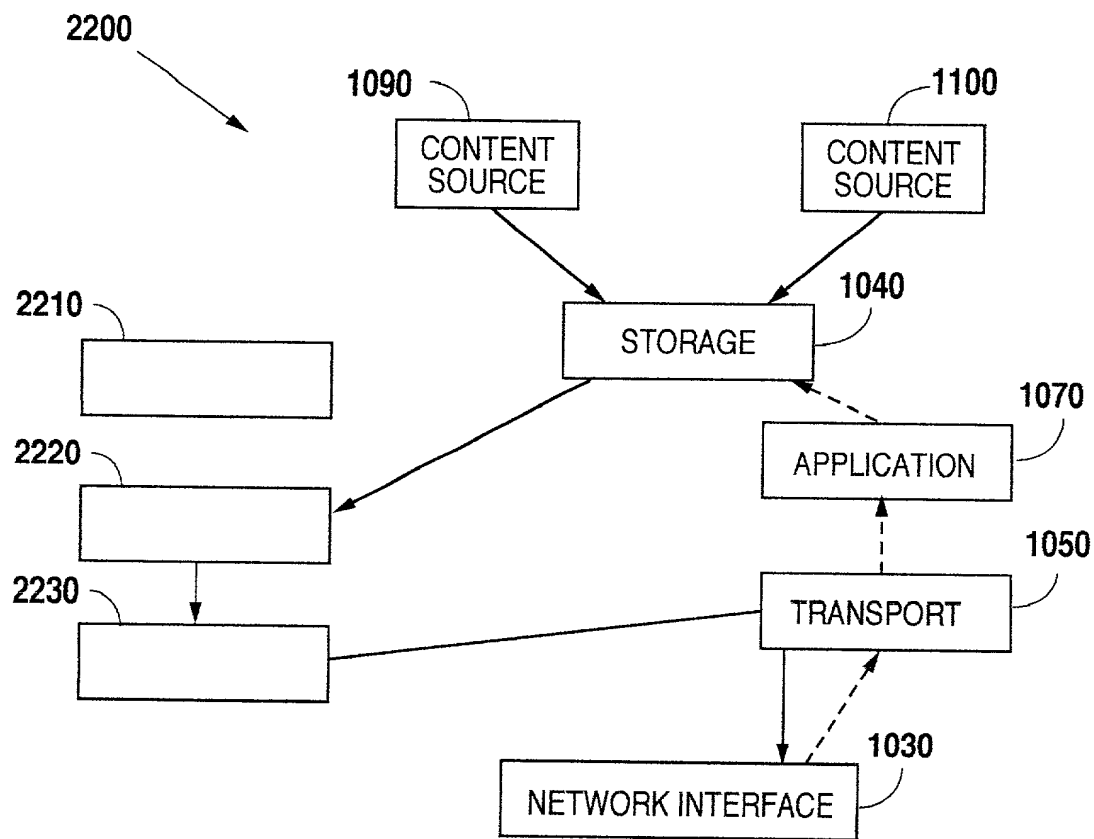


Fig. 15

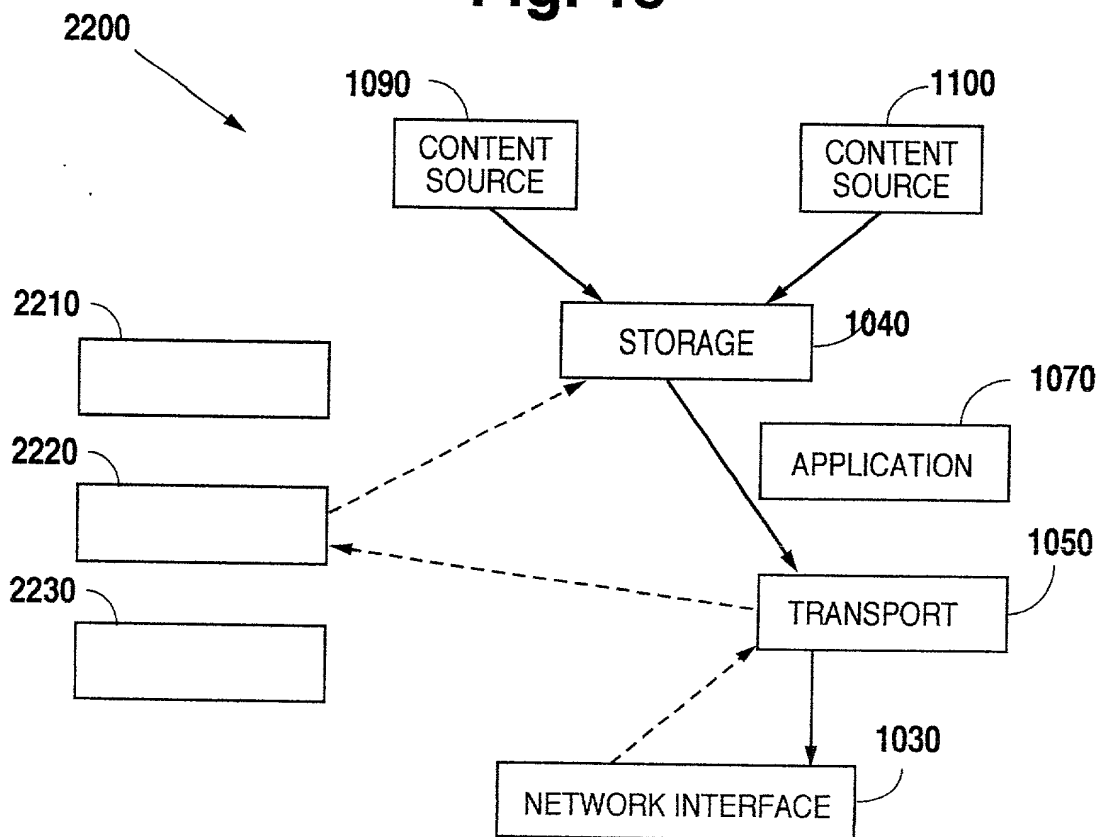


Fig. 16